PROCESSING SYSTEM WITH DIRECT MEMORY TRANSFER

FIELD OF THE INVENTION

[0001] The present invention relates generally to data processing systems and in particular the present invention relates to initiation of data processing systems.

BACKGROUND OF THE INVENTION

[0002] Processing systems, or computers, typically include a processor and a memory device as internal storage areas for the computer. The term memory identifies data storage that comes in the form of integrated circuit chips. While there are several different types of memory, DRAM (dynamic random-access memory) is traditionally used as the main memory in a computer environment. With the development of different RAM's, a high-speed synchronous-type DRAM is often used with the processor. The dynamic memory, however, cannot retain data in the absence of power. As such, computer system contains some non-volatile storage device. For example, a magnetic storage device or non-volatile memory can be used to store data and software.

[0003] During operation, the processor copies data from the non-volatile storage to the dynamic memory. That is, the data from the non-volatile storage is routed via the processor to the dynamic memory. This process consumes power, is time consuming, and consumes processor bandwidth.

[0004] For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a system and method of loading a volatile memory during power-up and reset operations in a more efficient manner.

SUMMARY OF THE INVENTION

[0005] The above-mentioned problems with processing systems and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[0006] In one embodiment, a processing system comprises a processor, a volatile synchronous memory device coupled to communicate with the processor, and a flash memory device coupled to communicate with the processor and the volatile synchronous memory device. The flash memory device transfers data directly to the synchronous memory device during power-up.

[0007] In another embodiment, a processing system comprises a processor, a volatile synchronous memory device coupled to communicate with the processor via a synchronous bus, and a flash memory device coupled to communicate with the processor via a serial bus and communicate with the volatile synchronous memory device via a direct bus. The flash memory device transfers data directly to the volatile synchronous memory device during power-up.

[0008] A processor system power-up method comprises detecting a power-up condition and providing a reset signal to a volatile synchronous memory, initiating a direct data transfer from a non-volatile memory to the volatile synchronous memory in response to the reset signal, and providing a system reset signal from the volatile synchronous memory to a processor.

[0009] Another processor system power-up method comprises detecting a power-up condition with a reset controller and providing a reset signal to a volatile synchronous memory, using the volatile synchronous memory, initiating a direct data transfer from a flash memory to the synchronous memory in response to the reset signal, and providing a system reset signal from the volatile synchronous memory to a processor after the data has been transferred.

[0010] A data transfer method comprises initiating a direct data transfer from a non-volatile memory to a volatile storage device, and transferring data from the non-volatile memory to the volatile storage device without control from an external processor

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 illustrates a block diagram of a memory device of an embodiment of the present invention; and

[0012] Figure 2 is a block diagram of a system of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0013] In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims.

[0014] Figure 1 illustrates a block diagram of a volatile memory device of an embodiment of the present invention. The memory device 100 includes an array of memory cells 102. In one embodiment, the memory contains multiple memory banks. The data stored in the memory can be accessed using externally provided location addresses received by address register 112. The addresses are decoded using row address decoder circuitry 114. To access an appropriate column of the memory, the received addresses are coupled to column decode circuitry 122. Data is input and output I/O buffer 128. Control 130 is provided to control the basic operations of the

memory device. A serial communication port 132 is provided to receive transferred data from a non-volatile storage device, as explained below. The memory has a reset input connection 134 to receive a reset signal used to begin a transfer operation. The memory also includes a reset signal output 136 to provide a reset signal to an external processor to indicate that the transfer is completed.

[0015] Referring to Figure 2, an embodiment of a processing system of the present invention is described. The system includes a central processing unit (CPU) 200, or processor, that is coupled to a synchronous memory bus 202 and corresponding volatile synchronous DRAM memory(ies) 204. The processor is also coupled to a synchronous flash memory 206. The synchronous DRAM (SDRAM) is coupled to the flash memory for copying data from the flash to the SDRAM during a power-up operation, as explained below. The volatile synchronous memory, in another embodiment, is a Rambus® DRAM (RDRAM). The present invention is not limited to volatile DRAM devices. Other embodiments can include a direct transfer to other volatile memory or storage devices.

[0016] A reset controller 210 is coupled to the SDRAM to initiate the memory upon power-up of the system. That is, when power is applied to the system, the reset controller provides a signal to the SDRAM indicating the supply voltage(s) has reached an acceptable level. In response to the reset signal, the SDRAM initiates a data transfer operation from the flash memory. This data transfer operation is direct from the flash to the SDRAM via a direct memory bus 212. After the data transfer is complete, the SDRAM provides a system reset signal 214 to the processor. The system reset signal indicates that the memory is ready for accessing.

[0017] In an alternate embodiment, the direct transfer from the non-volatile memory to the volatile storage device can be initiated after power-up. That is, the transfer can be initiated by the controller 200 and/or the volatile device 204 during normal operation periods.

[0018] The present invention allows the non-volatile memory contents to be directly loaded into the SDRAM without intervention by the processor. The processor, however, can be used to load and update the data in the flash memory. The flash memory of one embodiment can include features of a synchronous flash device, as described in U.S. Patent Application No. 09/627,682 filed July 28, 2000 and incorporated herein by reference. By directly loading the volatile memory, the overall system performance is improved. That is, the volatile memory is loaded faster than prior systems that use the processor to download the flash to the volatile memory. Further, less power is consumed by eliminating the processor from the data transfer operation. Isolating the non-volatile memory also reduces capacitive loading of the synchronous bus. As such, operating speeds of the synchronous bus may be increased.

CONCLUSION

[0019] A processing system has been described that allows direct data downloads from a non-volatile memory to volatile memory. During a power-up operation, the synchronous memory requests a direct transfer of data from the flash memory. Bypassing the synchronous communication bus allows for a faster transfer to the dynamic memory. Power and capacitive bus loading are also reduced. Once the synchronous memory is loaded, a system reset signal is provided to indicate that the memory is read.

[0020] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.